What is claimed is:

1. A data processing apparatus, comprising:

a first pipeline having a data cache and an instruction cache;

a second pipeline coupled to the data cache and the instruction cache; and

a data value prediction module coupled to the second pipeline.

2. The data processing apparatus of claim 1, further comprising:

a first instruction fetch module coupled to the first pipeline; and

a second instruction fetch module coupled to the second pipeline.

3. The data processing apparatus of claim 2, further comprising:

a branch predictor coupled to the first and second instruction fetch modules.

4. The data processing apparatus of claim 1, further comprising:

a first register file coupled to the first pipeline; and

a second register file coupled to the second pipeline.

5. The data processing apparatus of claim 1, wherein the first pipeline is included in a first processor, and wherein the second pipeline is included in a second processor.

6. The data processing apparatus of claim 1, wherein the first and second pipelines are included in a single processor.

7. The data processing apparatus of claim 6, wherein the data cache, the instruction cache, and the data value prediction module are included in the single processor.

8. The data processing apparatus of claim 1, further comprising:

a value prediction table coupled to the value prediction module.

9. The data processing apparatus of claim 1, further comprising:

a main memory coupled to the data cache, wherein the first pipeline may operate to store a data value to the main memory, and wherein the second pipeline may not operate to store the data value to the main memory.

10. The data processing apparatus of claim 1, further comprising:

a storage buffer coupled to the second pipeline.

11. The data processing apparatus of claim 1, further comprising:

a synchronization mechanism coupled to the second pipeline.

12. The data processing apparatus of claim 11, wherein the synchronization mechanism includes a misprediction counter.

13. A computer, comprising:

a first processor including a first pipeline having a data cache coupled to a memory, and an instruction cache;

a second pipeline coupled to the data cache and the instruction cache; and a data value prediction module coupled to the second pipeline.

14. The computer of claim 13, further comprising:

a second processor including the second pipeline.

15. The computer of claim 13, further comprising:

a bus coupled to the data cache and the memory, wherein the first processor includes the second pipeline.

16. The computer of claim 13, further comprising:

a value prediction table coupled to the value prediction module.

17. The computer of claim 13, further comprising:

a synchronization mechanism coupled to the second pipeline.

18. The computer of claim 17, wherein the synchronization mechanism includes a run-ahead counter.

19. The data processing apparatus of claim 13, further comprising:
a storage buffer coupled to the second pipeline.

20. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:
executing a plurality of instructions including a LOAD instruction using a first pipeline sharing an instruction cache and a data cache with a second pipeline;
calculating a predicted load value for execution of the LOAD instruction if a cache miss in the data cache results when the second pipeline executes the LOAD instruction before the first pipeline; and
continuing execution of the plurality of instructions using the second pipeline.

21. The article of claim 20, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:
counting a number of mispredictions occurring when the predicted load value is incorrect; and
restarting execution of the plurality of instructions by the second pipeline at a program counter value maintained by the first pipeline if the number of mispredictions is greater than or equal to a preselected threshold value.

22. The article of claim 20, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

counting a number of instructions included in the plurality of instructions which the second pipeline has executed ahead of the first pipeline; and

restarting execution of the plurality of instructions by the second pipeline at a program counter value maintained by the first pipeline if the number of instructions is greater than or equal to a preselected threshold value.

23. The article of claim 20, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

beginning execution of the plurality of instructions by the first and second pipelines at a same program counter value.

24. A method of processing data, comprising:

executing a plurality of instructions including a LOAD instruction using a first pipeline sharing an instruction cache and a data cache with a second pipeline;

calculating a predicted load value for execution of the LOAD instruction if a cache miss in the data cache results when the second pipeline executes the LOAD instruction before the first pipeline; and

continuing execution of the plurality of instructions using the second pipeline.

25. The method of claim 24, further comprising:

counting a number of mispredictions occurring when the predicted load value is incorrect; and

restarting execution of the plurality of instructions by the second pipeline at a program counter value maintained by the first pipeline if the number of mispredictions is greater than or equal to a preselected threshold value.

26. The method of claim 24, further comprising:

counting a number of instructions included in the plurality of instructions which the second pipeline has executed ahead of the first pipeline; and

restarting execution of the plurality of instructions by the second pipeline at a program counter value maintained by the first pipeline if the number of instructions is greater than or equal to a preselected threshold value.

27. The method of claim 24, further comprising:

beginning execution of the plurality of instructions by the first and second pipelines at a same program counter value.